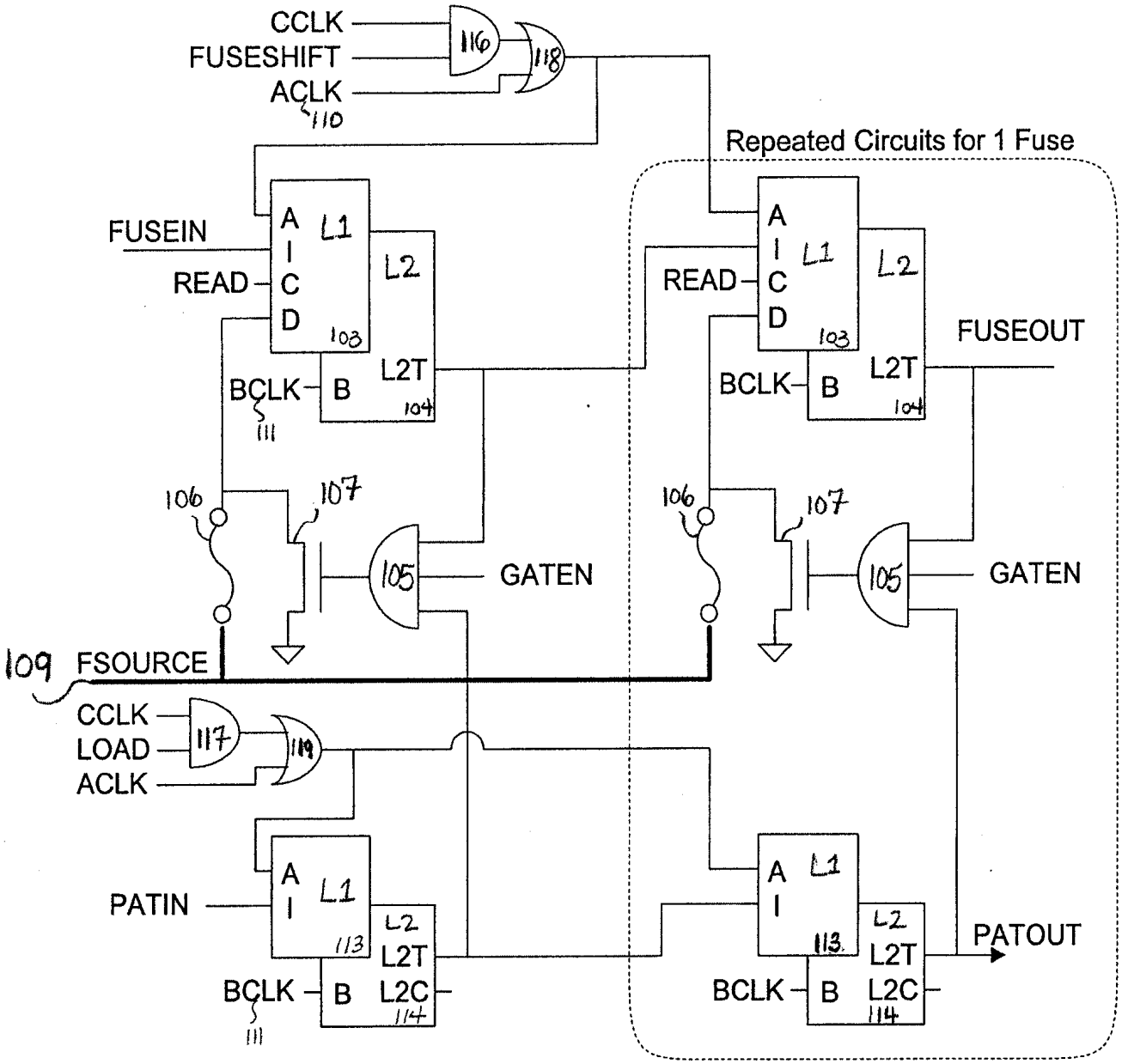

FIG. 1 (PRIOR ART)

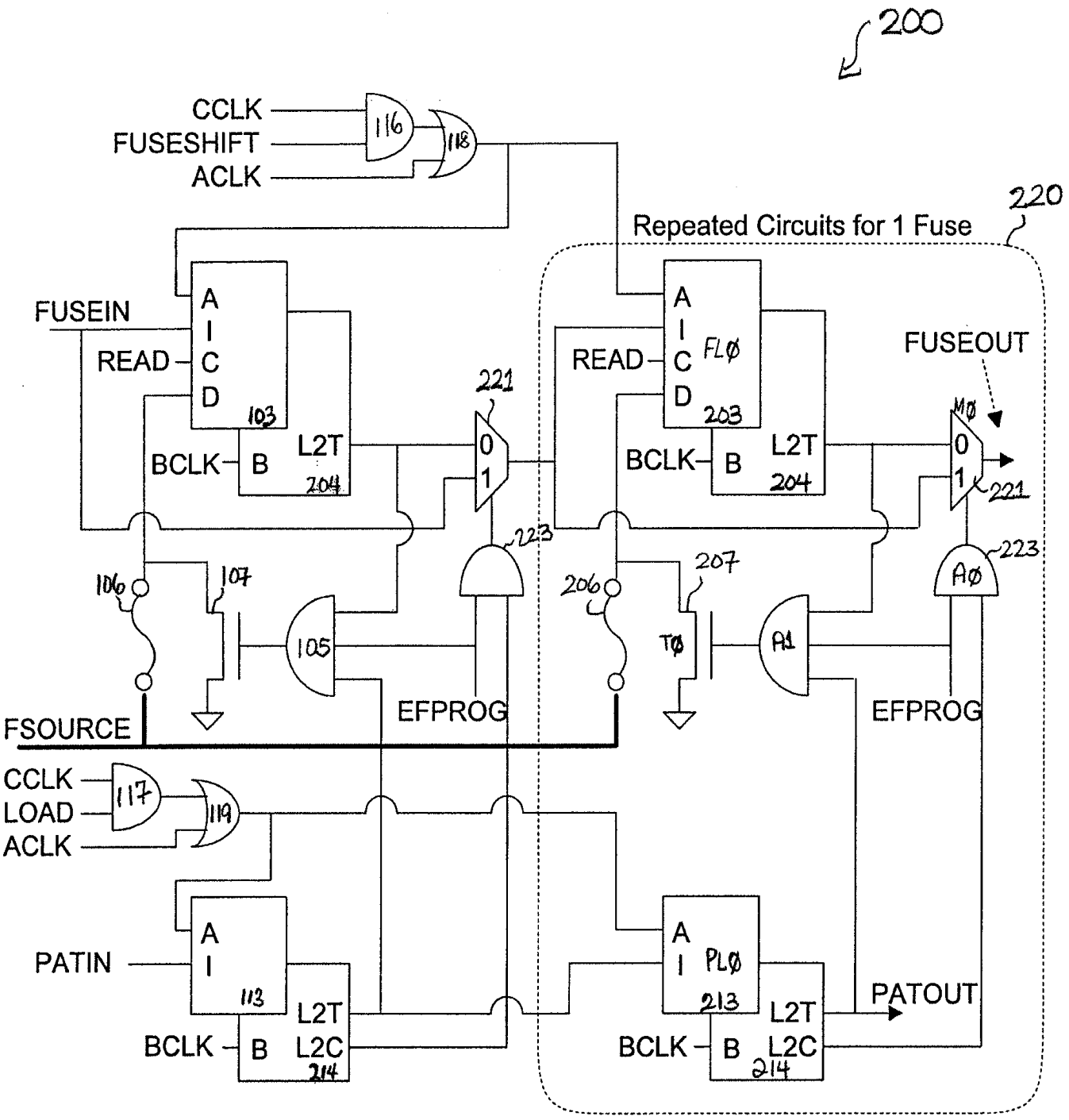
200
CCLK
FUSESHIFT
ACLK
116
118
220
Repeated Circuits for 1 Fuse
FUSEIN
READ
A
I
C
D
103
BCLK
B
L2T
204
221
0
1
223
106
107
105
EFPROG
FSOURCE
READ
FL0
203
FUSEOUT
M0
A0
A1
206
207
T0
CCLK
LOAD
ACLK
117
119
PATIN
113
L2C
214
PL0
213
PATOUT

FIG. 2

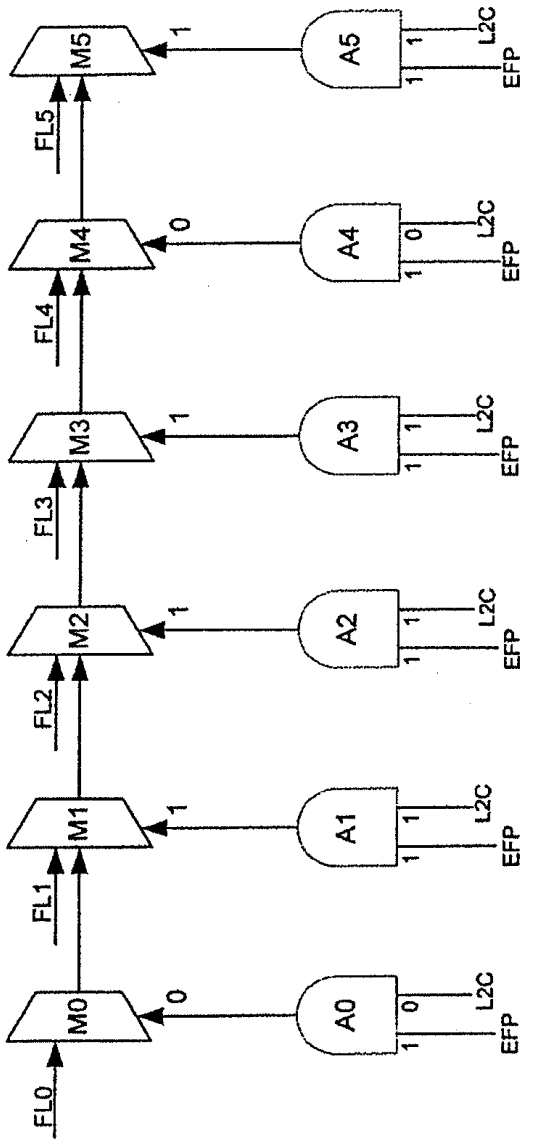

FIGURE 3A

	M0	M1	M2	M3	M4	M5
PRE-PROGRAMMED PATTERN LATCH	1	0	0	0	1	0
LOGIC SIGNALED	LATCH	MUX	MUX	MUX	LATCH	MUX
TEST TIME IN CLOCK CYCLES FOR SERIAL SHIFT (P.A)	1	1	1	1	1	1
TEST TIME IN CLOCK CYCLES WITH BYPASS	1	.01	.01	.01	1	.01

FIGURE 3B

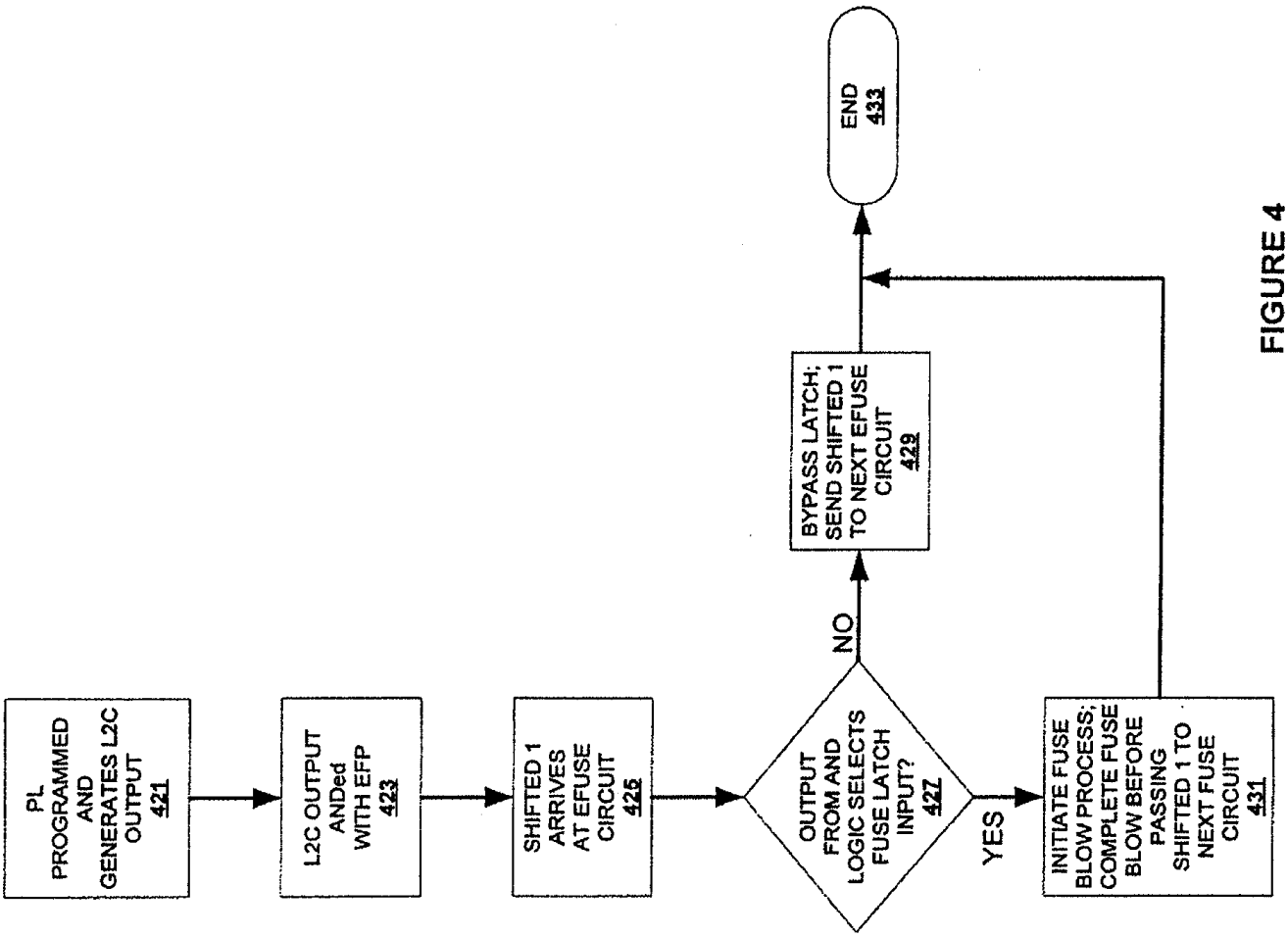
PL PROGRAMMED AND GENERATES L2C OUTPUT 421
L2C OUTPUT ANDed WITH EFP 423
SHIFTED 1 ARRIVES AT EFUSE CIRCUIT 425
OUTPUT FROM AND LOGIC SELECTS FUSE LATCH INPUT? 427
NO
YES
BYPASS LATCH; SEND SHIFTED 1 TO NEXT EFUSE CIRCUIT 429
INITIATE FUSE BLOW PROCESS; COMPLETE FUSE BLOW BEFORE PASSING SHIFTED 1 TO NEXT FUSE CIRCUIT 431
END 433

FIGURE 4